FIELD EFFECT TRANSISTORS

FET: CONTENTS

Principles of Operation

Models: DC, S.S.A.C. and SPICE

Applications: AC coupled S.S. Amplifiers

FET: NAMES

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET</td>
<td>Junction Field Effect Transistor</td>
<td>(Silicon)</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal - Oxide - Semiconductor FET</td>
<td>(Silicon)</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal - Semiconductor FET</td>
<td>(GaAs, III-V Semiconductor Alloys)</td>
</tr>
<tr>
<td>HEMT</td>
<td>High - Electron Mobility Transistor</td>
<td>(GaAs, III-V Semiconductor Alloys)</td>
</tr>
</tbody>
</table>
PRINCIPLES OF OPERATION AND CHARACTERISTICS of JFETs

\[ \rho = \frac{1}{\sigma} \] and \[ \sigma = e_n \mu_n + e_p \mu_p \] where

\( \rho \) - Resistivity (Ohms) \( \sigma \) - Conductivity (Siemens) \( e = 1.6 \times 10^{-19} \) Coulomb

\( n \equiv \text{electron density (cm}^{-3}\text{)} \) \( p \equiv \text{hole density (cm}^{-3}\text{)} \) \( \mu \equiv \text{mobility (cm}^2\text{Vs)} \)

For N - Type \( \sigma = e_n \mu_n \equiv e N_0 \mu_n \)

Current Density \( J \equiv \sigma \mathcal{E} \) Intrinsic Ohm’s Law \( I = GV \) Ohms Law

Current

\[ I_D = \int_{\text{area}} J.dA = JA \]

Electric Field

\[ \mathcal{E} = -\frac{dV}{dx} \quad \text{(or, } \mathcal{E} = -\nabla \Phi \text{ in 3 – Dimensions)} \]

\[ V_{DS} = -\int \mathcal{E}.dx = \mathcal{E}.L \]

\[ I_D = J.A = \sigma \mathcal{E}.A = \sigma \frac{V_{DS}}{L}.A = G.V_{DS} \]

or
\[ V_{DS} = \frac{1}{G} I_D = R \cdot I_D \]  

Ohm’s Law

where \( G = \sigma \frac{A}{L} \) or \( R = \sigma^{-1} \frac{L}{A} \)

Note that, for the N-type slab resistor shown above, majority carriers, i.e. electrons, dominate the current, therefore,

\[ I_D \approx \left( e N_D \mu_n \right) \frac{A}{L} V_{DS} \]

How can I make \( I_D \) be controlled by a variable other than \( V_{DS} \)?

Options: A, L and \( N_D \)

Which one of these can be controlled by a voltage or current? How?

Answer: A, through depletion around a PN junction => JFET

![Diagram of N-Channel JFET Cross Section](image)

Figure 2. Resistor I-V Chs.

Figure 3. N-Channel JFET Cross Section
Case (i). small \( V_{DS} \)

Obviously the smaller the cross sectional area the smaller the current flow becomes.
JFETs have been invented using this idea that current can be controlled by varying the cross section of a resistor made from an N-type semiconductor.

In JFETs the cross sectional area of a conducting channel is controlled by employing PN junctions. The facts that
(1) a PN junction creates a space charge layer around it which is depleted of carriers,
(2) the thickness of this layer increases with the reverse bias applied to it, and
(3) if the junction is made "one-sided" by heavily doping one side of the junction (P+) this depletion layer extends predominantly into the lowly doped side, are used.

When the two P+/N junctions in a P+/N/P+ sandwich structure are reverse biased their depletion layers take away thickness from the cross sectional area of the conducting N-type semiconductor channel in the middle, constricting electron flow and reducing (controlling/modulating) the current, $I_D$.

$p^+ \equiv$ heavily doped so voltage throughout these regions will be same in everywhere.

Total junction potential $\Delta V = V_{Bi} - V$ where $V = V_{GS}$

$I_G \approx 0$ since gate is reverse biased.

Power Controlled: $P_D = I_D \cdot V_{DS}$

Figure 4. N-Channel JFET for small $V_{DS}$
Controlling Power: \( P_G = I_G \cdot V_{GS} \approx 0 \)

\[ \Rightarrow \quad \text{Power Gain} = \frac{P_D}{P_G} \approx \text{Infinite (potentially)} \]

1. What if \( V_{GS} < -|V_{PO}| \)?

- \( I_D \) remains to be zero.
- \( G \) remains to be zero.
- \( R \) remains to be infinite.

2. What if \( V_{GS} > 0 \), forward biasing?

Do not forward bias it. It will diminish the power gain.

Keep \( V_{GS} < 0.6 - 0.7 \) V to prevent turning on of the gate junction (for Silicon made JFETs).

3. What if \( V_{GS} < -\text{Gate Breakdown Voltage} \)?
Breakdown! large currents flow with no control. The device stops working properly. Possibly damaged by high current.

**JFET I-V CHARACTERISTICS**

\[ I_D = \frac{e N_D \mu n}{L} \ z \ (2 \ a - 2 \ d) \ V_{DS} \]

where the depletion layer thickness,

\[ d = d \ (V_{Bi} - V_{applied}) = \sqrt{\frac{2 \ e \ (V_{Bi} - V_{applied})}{eN}} \]

\[ V_{applied} = (\text{Gate} \ - \ \text{to} \ - \ \text{Channel}) \ \text{bias} = \begin{cases} V_{GS} & \text{at source side of the channel, } V_{GS} < 0 \\ V_{GS} - V_{DS} & \text{at drain side of the channel, } V_{GS} < 0 \end{cases} \]

Therefore, \((d)_{\text{source side}} < (d)_{\text{drain side}}\)

(Nonuniform Cross Sectional Area) and \(I_D = \text{constant, independent of position}\)
Therefore, current density increases from Source to Drain, making the horizontal gradient of channel potential, i.e., channel electric field nonuniform along the channel.

Solutions to the mathematical problem is found in Streetman's or other textbooks (ELE 262)

\[ I_D = \frac{Z\mu_n e^2 N^2 a^3}{\varepsilon L} \left( \frac{V_{DS}}{V_{PO}} \right) - \left( \frac{2}{3} \left( \frac{V_{DS} + V_{GS} + V_{BI}}{V_{PO}} \right) \right)^{\frac{3}{2}} + \frac{2}{3} \left( \frac{V_{GS} + V_{BI}}{V_{PO}} \right)^{\frac{3}{2}} \]

This nonlinear equation for \( I_D \) is applicable to JFETs with uniform channel doping, only. It is nonlinear and too complicated to use in the analysis and design of JFET circuits.

For nonuniformly doped JFETs (and for uniformly doped channel JFETs as well) a simpler square law empirical model (which is best fitted to measured I-V data) described by the equations below is used for hand calculations and in design.

\[
I_D = \begin{cases} 
0 & \text{Cut-off} \quad V_{GS} < -|V_{PO}| \\
I_{DSS} \left[ \frac{2(V_{GS} - V_{PO}) V_{DS} - V_{DS}^2}{(V_{PO})^2} \right] & \text{Linear} \\
I_{DSS} \left[ 1 - \frac{V_{GS}}{V_{PO}} \right]^2 & \text{Saturation}
\end{cases}
\]

Note that if the reverse potential across the depletion layer at the drain side becomes equal to a value, \((V_{GS} - V_{DS}) = -|V_{PO}|\), the drain end of the channel gets "pinched-off", the shape of the conducting channel becomes same as a bullet with a sharp tip. If VDS is increased beyond this point, the shape remains the same, resulting in the saturation of drain current.
The above I-V relationship applies to uniformly doped channel JFETs as well as nonuniformly doped channel JFETs. Its modified forms are also used for other FETs, namely, MESFETs, HEMTs and MOSFETs.

**Linear**
\[(V_{GS} - V_{DS}) > -|V_{PO}|\]

**Saturation**
\[(V_{GS} - V_{DS}) < -|V_{PO}|, \quad \text{(Drain side of the channel is pinched off)}\]

**Proof of \(I_D(V_{GS})\) in saturation:**

At the transition point: \(V_{GS} - V_{DS} = V_{PO}\) or, \(V_{DS} = V_{GS} - V_{PO}\)

Substitute this in \(I_D(V_{GS}, V_{DS})\)

\[
I_D = \frac{I_{DS}}{|V_{PO}|^2} \left[ 2(V_{GS} - V_{PO})(V_{GS} - V_{PO}) - (V_{GS} - V_{PO})^2 \right]
\]

\[
I_D = \frac{I_{DSS}}{|V_{PO}|^2} (V_{GS} - V_{PO})^2
\]
\[ I_D = I_{DSS} \left( \frac{V_{GS}}{V_{PO}} - 1 \right)^2 = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{PO}} \right)^2 \quad \text{(In saturation)} \]

**SYMBOLS**

- **MODELS**

As long as \( V_{GS} \) reverse biases the gate junction with negligible leakage current the JFET can be represented with an open circuit at the Gate-Source and a dependent current source at the Drain-Source terminal as shown in Figure 10.

\[ \text{where } I_G = 0 \text{ and} \]

Figure 9. N-Channel JFET Bias in Normal Operation

Figure 10. P-Channel JFET Bias in Normal Operation

Figure 10. DC Model of N-JFET
\[
I_D = \begin{cases} 
0 & \text{Cut-off} \quad V_GS < -|V_{PO}| \\
\frac{I_{ss}}{|V_{PO}|} [2(V_GS - V_{PO})V_D - V_D^2] & \text{Linear} \quad V_GS > -|V_{PO}| \text{ and } V_D < V_GS - V_{PO} \\
I_{DS} [1 - \frac{V_GS}{V_{PO}}]^2 & \text{Saturation} \quad V_GS > -|V_{PO}| \text{ and } V_D > V_GS - V_{PO}
\end{cases}
\]

**SMALL SIGNAL AC:**

The small signal variations in drain and gate currents around an operating point of \( I_{DQ} \) (\( V_{DSQ}, V_{GSQ} \)) and \( I_{GQ} \approx 0 \) are,

\[
\Delta i_D = \left( \frac{\partial i_D}{\partial V_GS} \right)_Q \Delta V_GS + \left( \frac{\partial i_D}{\partial V_D} \right)_Q \Delta V_D \quad \text{and} \quad \Delta i_G = 0 \quad \text{where},
\]

\[
g_m = \left( \frac{\partial i_D}{\partial V_GS} \right)_Q \quad \text{Drain Transconductance: Gate Voltage \rightarrow Drain Current}
\]

\[
g_{ds} = \left( \frac{\partial i_D}{\partial V_D} \right)_Q \quad \text{Drain Conductance: Drain Voltage \rightarrow Drain Current}
\]

This implies a simple small signal AC equivalent circuit shown in Figure 11. below.

![Small Signal AC Equivalent Circuit](Figure 11. SSAC Model of N-JFET)

**IN SATURATION:**

In most amplifier applications JFETs are operated in their saturation region. In saturation,

\[
\left( \frac{\partial i_D}{\partial V_D} \right)_Q = 0 \quad \Rightarrow \quad g_{ds} = 0 \quad \text{and},
\]
\[
\left( \frac{\partial i_D}{\partial V_{GS}} \right)_{SAT} = \left( \frac{\partial}{\partial V_{GS}} \left[ I_{DSS} \left( 1 - \frac{V_{GS}}{V_{PO}} \right)^2 \right] \right)_Q \Rightarrow \quad g_m = \left( 2 I_{DSS} \left( 1 - \frac{1}{V_{PO}} \right) \left( 1 - \frac{V_{GS}}{V_{PO}} \right) \right)_Q
\]

Note that \( g_m \) varies linearly with \( V_{GSQ} \). This property can be used to design amplifiers with electrically variable gains (voltage-controlled-amplification).

- **A SIMPLE SSAC JFET AMPLIFIER:**

![Diagram of a simple N-JFET amplifier](image-url)
\[
\Delta V_{\text{out}} = -g_m \Delta V_{\text{GS}} (g_{\text{ds}}^{-1} \parallel R_D \parallel R_L) \\
\Delta V_{\text{GS}} = \Delta V_{\text{in}} = v_{\text{gs}} \\
\Delta V_{\text{out}} = V_{\text{out}} \\
A_V = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = -g_m \left( g_{\text{ds}}^{-1} \parallel R_D \parallel R_L \right)
\]

where \( g_m \) is linearly dependent on \( V_{\text{GSQ}} = V_{\text{GG}} \), as shown before.

APPLICATION: Automatic Volume Control in AM / Short Wave Receivers, where loudspeaker voltage is rectified and used to push \( V_{\text{GSQ}} \) toward \( V_{\text{PO}} \) when the sound volume increases.
In a real JFET two major deviations from our previously developed model are found.

1. Breakdown

\[ V_{DG} = |V_{DS}| + |V_{GS}| = V_{DS} \text{ positive, } V_{GS} \text{ negative} \]

\[ |V_{DS}|_{\text{Breakdown}} = |V_{DG}|_{\text{Breakdown}} - |V_{GS}| \]

\[ |V_{DS}|_{\text{Breakdown}} \text{ varies with } |V_{GS}| \text{ since } |V_{DG}|_{\text{Breakdown}} \text{ is a constant junction breakdown voltage.} \]

2. Channel Length Modulation \( \equiv \lambda \) (Non-zero slope in saturation)

\[
I_D = \begin{cases} 
0 & \text{Cut-off} \\
\frac{I_{DSS}}{|V_{PO}|} \left[2(V_{GS} - V_{PO})V_{DS} - V_{DS}^2\right](1 + \lambda V_{DS}) & \text{Linear } V_{GS} > -|V_{PO}| \text{ and } V_{DS} < V_{GS} - V_{PO} \\
I_{DSS} \left[1 - \frac{V_{GS}}{V_{PO}}\right]^2(1 + \lambda V_{DS}) & \text{Saturation } V_{GS} > -|V_{PO}| \text{ and } V_{DS} > V_{GS} - V_{PO} 
\end{cases}
\]
(I_D)_{\text{SATURATION}}:

![Graph showing transfer characteristics in saturation with curves for IDSS (1 + \lambda VDS1) and IDSS (1 + \lambda VDS2).]

**Figure 16. Transfer Characteristics in Saturation**

- **IMPROVED SMALL SIGNAL EQUIVALENT PARAMETERS IN SATURATION**

![Diagram of SSAC model in saturation with symbols gm, vgs, 1/gd = rds.]

**Figure 17. SSAC Model in Saturation**
Figure 18. Effect of Lambda on $g_m$

$$g_m = \left( \frac{\partial i_D}{\partial v_{GS}} \right) \text{V}_{DS} = \text{V}_{DSQ} = \text{constant}$$

$$g_m = \frac{2 \text{I}_{DSQ}}{(-v_{PO}) \left(1 - \frac{v_{GSQ}}{v_{PO}} \right)} \left(1 + \lambda v_{DSQ} \right)$$

Figure 19. Definition of Lambda

$$g_{ds} = \left( \frac{\partial i_D}{\partial v_{DSQ}} \right)_Q = \lambda \text{I}_{DS} \left(1 - \frac{v_{GSQ}}{v_{PO}} \right)^2 = \lambda \text{I}_{DSQ} \left/ \left(1 + \lambda v_{DSQ} \right) \right.$$
TEMPERATURE EFFECTS

1. Thermally more stable than BJT:

   $I_{DSS}$ is proportional to $\mu$ which decreases as temperature increases. Therefore, $I_D$ can not run off at high temperatures.

   In BJTs, however, $\beta$ (+1 %/C) and $I_{CEO}$ (doubles every 7°C) increase with temperature, therefore, BJTs are vulnerable to thermal runaway of their operating point currents.

2. Pinch – Off Voltage decreases in magnitude when temperature increases.

   $$\frac{d |V_{po}|}{dT} \sim H - 2mV/2.5mV per ^\circ C$$