7. DESIGN OF AC-COUPLED BJT AMPLIFIERS FOR MAXIMUM UNDISTORTED VOLTAGE SWING

Figure 1. AC coupled common emitter amplifier circuit

The DC Load Line

\[ V_{CC} = R_C I_{CQ} + V_{CEQ} + R_E I_{EQ} \]

\[ I_{EQ} = I_{CQ} + I_{BQ} \quad I_{CQ} = \beta_{EFF} I_{BQ} \]

\[ I_{EQ} = \frac{\beta_{EFF} + 1}{\beta_{EFF}} I_{CQ} \approx I_{CQ} \]

These equations lead to a linear relationship between \( I_{CQ} \) and \( V_{CEQ} \) which is imposed on the DC operating point of the transistor by the circuit.

\[ V_{CC} = \left( R_C + R_E \frac{\beta_{EFF} + 1}{\beta_{EFF}} \right) I_{CQ} + V_{CEQ} \quad \text{or,} \]

\[ I_{CQ} = \left( V_{CC} - V_{CEQ} \right) \left[ R_C + R_E \left( 1 + \frac{1}{\beta_{EFF}} \right) \right] \]

the "DC Load Line Equation"
Slope of DC Load Line:
\[
\frac{\Delta I_{CQ}}{\Delta V_{CEQ}} = -\left[R_C + R_E \left(1 + \frac{1}{\beta_{EFF}}\right)\right]^{-1} \approx -[R_C + R_E]^{-1}
\]

Figure 2. shows the DC load line of the circuit drawn on the collector characteristics of an NPN transistor.

Assumptions:
1. The capacitors are all large enough to hold the voltage across their terminals constant during the signal's period,
2. Therefore, the operating point \(Q(I_{CQ}, V_{CEQ})\) remains constant independent of the amplitude of the signal fluctuations in currents and voltages.

If that is the case, the capacitors in the circuit can be taken to behave like DC voltage sources as shown in Figure 3.

**AC Load Line**

\[
\Delta I_C = f(\Delta V_{CE}) \quad \Delta V_{CE} = \Delta V_{OUT}
\]
Figure 3. Behavioral equivalent of the common emitter stage with very large capacitors

\[ \Delta v_{CE} = \Delta v_C - \Delta v_E \quad \text{and} \quad \Delta i_C = \Delta i_{RC} + \Delta i_{RL}, \quad \Delta v_E = 0 \quad \text{constant} \]

\[ \Delta i_{RC} = \Delta \left( \frac{v_{CC} - v_C}{R_C} \right) = -\frac{\Delta v_C}{R_C} \]

\[ \Delta i_{RL} = -\frac{\Delta v_{OUT}}{R_L} \quad \Delta v_{OUT} = v_C - V_{CQ} = \Delta v_C \quad \Rightarrow \Delta i_{RL} = -\frac{\Delta v_C}{R_L} \]

But, \[ \Delta v_C = \Delta (v_{CE} + V_{EQ}) = \Delta v_{CE} \quad \therefore \quad \Delta i_C = -\frac{\Delta v_{CE}}{R_C} - \frac{\Delta v_{CE}}{R_L} \]

or, \[ \Delta i_C = -\left( \frac{1}{R_C} + \frac{1}{R_L} \right) \Delta v_{CE} \quad \text{which defines the "AC load line"} \]

Slope of AC Load Line \[ \equiv \left( \frac{1}{R_C} + \frac{1}{R_L} \right) \equiv \frac{1}{(R_C \parallel R_L)} \]

For smaller signals the resistance seen by the transistor at its collector can be found by employing the small sig ac equivalent of the circuit (given in Figure 4) is the same, i.e. \((R_C \parallel R_L)\), which confirms the slope calculation above.
In Figure 2, both AC and DC load lines are shown as drawn on the collector characteristics of an NPN transistor. Note that both of the lines have to pass through the operating point, Q. The AC load line defines the range of collector the current and voltage swings that can take place around the operating point, the range limited on the left by the saturation region of the transistor characteristics and on the right by its cut-off point. If the swings exceed these limits, the waveform is clipped, creating severe distortion in the amplified signal. The undistorted (unclipped) voltage swing is restricted to $\Delta v_{\text{MAX}}^-$ and $\Delta v_{\text{MAX}}^+$ around the operating point. (See Figure 5.)

1. $\Delta v_{\text{MAX}}^+ = \Delta v_{\text{MAX}}^-$
2. $\Delta v_{\text{MAX}}^- = R_{\text{AC}} I_{\text{CQ}}$  

AC load line resistance $\equiv R_{\text{AC}} = (R_C \parallel R_L)$

$\Delta v_{\text{MAX}}^- = V_{\text{CEQ}} - V_{\text{CESAT}}$
Figure 5. AC load line and the maximum undistorted output swing
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Rewriting the maximum peak undistorted swing conditions from above and using the condition of equal symmetric undistorted swings around the operating point an equation for maximum swing can be derived as shown below.

1. \( \Delta V_{\text{MAX}} = \Delta V_{\text{MAX}^+} = \Delta V_{\text{MAX}^-} \)
2. \( \Delta V_{\text{MAX}} = R_{\text{AC}} I_{\text{CQ}} \quad \rightarrow \quad I_{\text{CQ}} = \frac{\Delta V_{\text{MAX}}}{R_{\text{AC}}} \)
3. \( \Delta V_{\text{MAX}} = V_{\text{CEQ}} - V_{\text{CESAT}} \quad \rightarrow \quad V_{\text{CEQ}} = \Delta V_{\text{MAX}} + V_{\text{CESAT}} \)
4. \( V_{\text{CC}} = V_{\text{EQ}} + V_{\text{CEQ}} + R_C I_{\text{CQ}} \)

Equations (2) and (3) when substituted in Equation (4)

\[ V_{\text{CC}} = V_{\text{EQ}} + \Delta V_{\text{MAX}} + V_{\text{CESAT}} + \Delta V_{\text{MAX}} \cdot \frac{R_C}{R_{\text{AC}}} \]

(5.a) \[ \Delta V_{\text{MAX}} \left(1 + \frac{R_C}{R_{\text{AC}}}\right) = V_{\text{CC}} - V_{\text{EQ}} - V_{\text{CESAT}} \]

or,

(5.b) \[ \Delta V_{\text{MAX}} \left(2 + \frac{R_C}{R_L}\right) = V_{\text{CC}} - V_{\text{EQ}} - V_{\text{CESAT}} \]

since \( \frac{1}{R_{\text{AC}}} = \frac{1}{R_C} + \frac{1}{R_L} \)

Equations 5.a and 5.b can be used as design guides to achieve a specified amount of symmetric undistorted voltage swings at the output of a common-emitter amplifier.

Note that the maximum undistorted peak swing, \( \Delta V_{\text{MAX}} \), cannot be greater than \%50 of \( V_{\text{CC}} \) even under the most favorable conditions of no load and no emitter drop, \( V_{\text{EQ}} \).