Senior Design Project Report

on

Silicon P-N Junction Photodiode Fabrication

By Tho Thi Snow

Project Advisor: Prof. Mustafa G. Guvench

Submitted to: Prof. Mustafa G. Guvench

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University of Southern Maine

Department of Electrical Engineering

Table of Content:

I. Objective of project

The objective of this project was to apply the theoretical knowledge about silicon integrated circuit fabrication processes to fabricate a Si P-N junction Photodiode that corresponded to Red 632.8nm HeNe Laser or Red 660nm LED.

II. Fabrication Processes:

Calculations for Fabrication parameters were shown in Mathematica file named "Calculations for fabrication parameters.nb"

Silicon integrated circuit fabrication processes involved in creating a silicon p-n junction photodiode in this project were oxide growth, dopant diffusion and vacuum metallization. Full fabrication processes should have included photolithography process; however, this process was omitted due to equipment's unavailability. A cross sectional structure of a Si p-n junction photodiode was shown in figure 1.

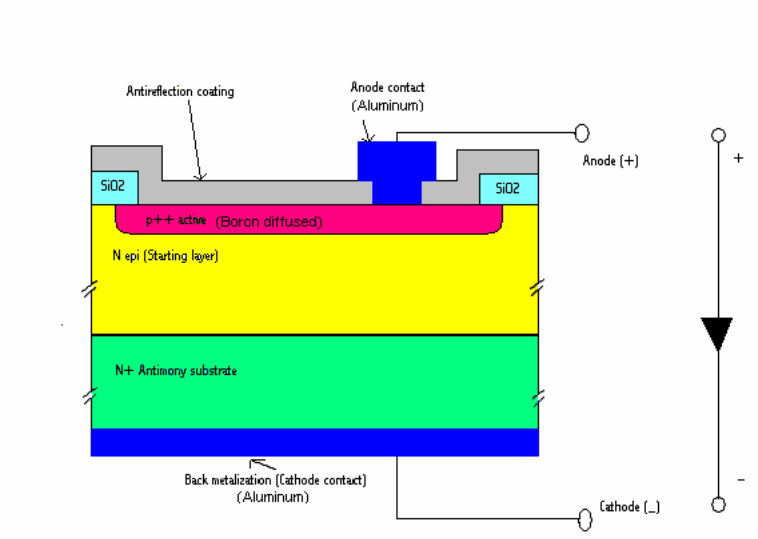

Figure 1: Cross sectional structure of a Si p-n junction photodiode

With the constrain due to equipment's unavailability as mentioned above, the real fabrication process still carried out in a normal sequence, i.e. the oxidation step first (as an experiment), then boron doping and diffusion, after that etching, vacuum metallization, and finally with antireflection coating.

The materials used in the fabrication processes were:

- Starting wafer: 4-in diameter N-type doped, <111> Silicon Wafer
- Dopant: Boronsilicafilm , $C_0 = 5 \times 10^{20}$ cm^{-3} (Emulsitone company)
- Diffusion gas: Nitrogen (N2)
- Etchant: Buffered Hydrofluoric acid (BHF)
- Metal: 0.5mm diameter Aluminum wire
- Others: De-ionized (DI) water…

A. Oxide Growth

Furnace control units

Hot furnace tube @1050 C

Figure 2: Oxidation system

Silicon and oxygen were very active. Even at room temperature, when silicon wafer was exposed to air, silicon combined with oxygen in air forming a thin oxide layer of ~10→ 20 Angstroms. Therefore, thermal oxidation of silicon was easily achieved by heating the wafer to a high temperature, typically in the range from 900 to 1200 C, in an atmosphere containing either pure oxygen or water vapor. In order for oxidation to continue occurring after a layer or silicon dioxide had been formed on the wafer surface,

oxygen must reach the silicon interface. Luckily, this was not an issue since at these high temperatures, oxygen and water vapor diffused easily through silicon dioxide. As the oxide grew, oxygen must pass through more and more oxide. As a results, the growth rate decreased as time went on. The chemical reaction occurring at the silicon surface was:

For dry oxygen:

$Si + O2 \rightarrow SiO2$

For wafer vapor:

$Si + 2H2O \rightarrow SiO2 + 2H2$

The grown oxide thickness was calculated based on the following function:

$$t = \frac{X_0^2}{B} + \frac{X_0}{\frac{B}{A}} - \tau$$

- where X0 = thickness of the oxide at a given time

- B = parabolic rate constant
- B/A = linear (growth) rate constant
- $\left(\tau = \frac{X_i^2}{B} + \frac{X_i}{\frac{B}{A}} \right)$

  τ = time which would have been required to grow the initial oxide Xi.

Parabolic rate constants, B, of <100> Si wafers were different from those of <111> Si wafers. So were linear rate constants, B/A. Parabolic and linear rate constants varied with temperature as well. Based on available data listed in reference [2], written functions shown below would be used to calculate dry and wet oxidation times for available wafers for this project, i.e. 4 in-diameter, N-type doped, <111> Si wafers.

Parabolic and linear rate constants were the denominators of the first and the second term of the function, respectively.

```
(*The following functions calculate oxiadion time for <111> Silicon,
 Xi (in μm) is the initial existing oxide thichness,
 X0 (in μm) is the thickness of the oxide layer to be grown,
 T (in °C) is the oxidation temperature*)
timewetoxide[Xi_, X0_, T_] := X0^2/(386 * Exp[-0.78/(8.617*10^-5 (T+273))]) + X0/(1.63 * 10^8 * Exp[-2.05/(8.617*10^-5 (T+273))]) -
    (Xi^2/(386 * Exp[-0.78/(8.617*10^-5 (T+273))]) + Xi/(1.63 * 10^8 * Exp[-2.05/(8.617*10^-5 (T+273))]))(*hours*);
timedryoxide[Xi_, X0_, T_] := X0^2/(772 * Exp[-1.23/(8.617*10^-5 (T+273))]) + X0/(6.23 * 10^6 * Exp[-2.00/(8.617*10^-5 (T+273))]) -
    (Xi^2/(772 * Exp[-1.23/(8.617*10^-5 (T+273))]) + Xi/(6.23 * 10^6 * Exp[-2.00/(8.617*10^-5 (T+273))])) -
    (0.025^2/(772 * Exp[-1.23/(8.617*10^-5 (T+273))]) + 0.025/(6.23 * 10^6 * Exp[-2.00/(8.617*10^-5 (T+273))]))(*hours*);
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These equations were used to calculate parameters for the oxidation process. Based on calculated results, either wet or dry oxygen was chosen. Since a very thick oxide wasn't necessary for this project, all oxide in this project was grown in air, which could be considered as in dry oxygen.

Actual steps in oxidation process were:

- Place wafers on to the oxidation boat
- Push the boat in to the middle of the furnace tube
- Use furnace controller, i.e. computer, to program the temperature of the furnace tube to ramp up to oxide growing temperatures (1000 and 1050^{0}C in this project)
- Pull wafers out after a desire oxidation time.

The oxidation experiment was carried out on one 4-in diameter, N-type doped, <111> Si wafer. It was oxidized in air twice: 1hour at 1000 C and then 1 hour at 1050 C.

B. Dopant (Boron) Diffusion

Since a heavily P-type doped was wanted, boron was chosen as the dopant, and it was doped to the wafer at the solid-solubility limit for boron, which was the maximum limit that silicon could absorb boron. The diffusion was carried out using the same system as the one used to grow oxide as shown in figure 2.

Processing steps:

• Deposit Boronsilicafilm solution on top of wafer

• Dry in oven at 150^0C for ~15 min

• Load on to diffusion boat, then push the boat to the middle of furnace tube

• Turn on diffusion gas and the furnace, ramp up time = 90 min. to reach diffusion temperature of 1050^0C

• After a wanted diffusion time, pull the wafer out of the furnace tube

C. Etching

The etching step was carried out at room temperature after boron diffusion step. The back oxide, which existed on the starting wafer, and the doping solution film left on the surface of the wafer, both needed to be removed before depositing contact metal electrodes. Wet chemical etching method - an isotropic process - was used for all etchings in the fabrication process. The wet etchant used was buffered hydrofluoric acid solution (BHF), which was the etching solution consisting of hydrofluoric acid and a buffering agent, ammonium fluoride (NH4F), added to the etching solution to prevent depletion of the fluoride ions in the oxide etch. BHF chemically reacted with etched films to form water-soluble byproducts or gases. The overall chemical reaction for SiO2 etching was:

$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

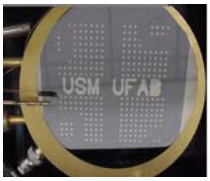
(H_2SiF_6 was a water-soluble complex)

At room temperature, the etch rate in BHF ranged from 100 A^0 to 1000 A^0. The etch rate depended on temperature, the density of the silicon dioxide film, and also on the type of oxide present; for example oxides grown in dry oxygen etched more slowly than those grown in the present of water vapor. BHF etched borosilicate glass forming from the remaining doping solution on the front doping surface of the wafer, at a slower rate than that of silicon dioxide film. Since there were many factors as mentioned determined the etch rate, and the information of most of those factors weren't available or couldn't be determined, the etch rate of BHF for this project process was not known exactly. However, the etching times could be determined based on the occurrence of a hydrophobic condition (i.e. etching solution washed away from the etched surfaces) on the wafer signaling the completion of the etch step. The recorded etching times were from 3 to 4 minutes for the back oxide and about 12 minutes for the borosilicate glass on the doping surface of the wafer. After the wafer went through the chemical etching, it was rinsed with de-ionized water and blew dry with nitrogen gas. Then, it was ready for the vacuum metallization deposition step.

D. Vacuum Metallization Deposition

Vacuum Deposition System used in Al vapor deposition.

Chamber environment = air
Chamber Pressure = 10^{-6} torr
Current = 40 -> 50 A



Tested wafer after Al deposition process

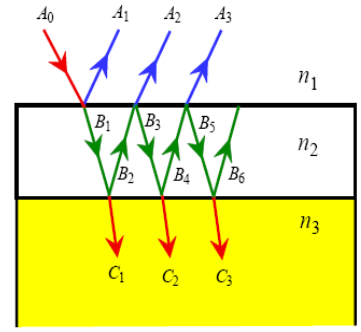
Figure 3: Vacuum deposition system

After the wafer went through the etching step, both front and back surface of the wafer were clean and ready for depositing contact metal electrodes for the device. Aluminum was used as the metal material in the metallization process. It was deposited on the surface of the wafer through the mask by evaporation deposition method. The deposition was carried out in the vacuum chamber of a basic vacuum deposition system in the Micro-Fabrication at the University of Southern Maine. Following the etching step, the wafer was placed on top of metal mask sitting on the rack inside the vacuum chamber. Pressure in the chamber was lower down to the processing chamber pressure of $\sim 2*10^{-6}$ torr by a mechanical pump and a high-vacuum pump of the vacuum deposition system. The vacuum environment was air. The tungsten boat holding a 10cm of 0.5 diameter aluminum wire was placed about 10 cm below the wafer and resistively heated by passing an alternate current (AC) through it. Aluminum on the tungsten boat melt and then vaporized at a current in the range from 40 amperes to 50 amperes. The aluminum vapor came up through the mask and sticked and condensed on the exposed surface of the wafer. The same deposition method was applied for forming both anode contact (i.e. boron p++ active layer/ front surface contact) and cathode contact (N++ antimony doped substrate/ back contact). The wafer then went through the final processing step that was antireflection coating.

E. Antireflection Coating

When light was incident on the surface of a semiconductor, it became partially reflected. A photodiode would need as much light transmitted into the device as possible to convert to electrical energy. An antireflective coating therefore was needed. The ideal

material for antireflective coating on silicon diodes operating in air was the one that had a refractive index of 1.87 (i.e. n ideal anti. $= \sqrt{n \text{ air} * n \text{ silicon}} = \sqrt{1 * 3.5} = 1.87$).



Thin film coating of refractive index n_2 on a semiconductor device

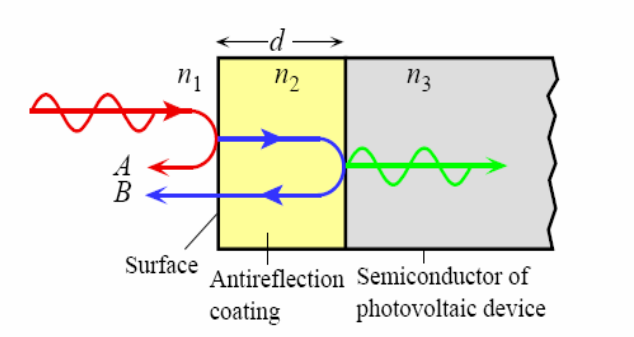


Illustration of how an antireflection coating reduces the reflected light intensity

Figure 4: Antireflection coating on a semiconductor device

Even though silicon dioxide, which had an index of reflection of 1.46 closed to the ideal value of 1.87, was not the optimal material for antireflection coating on the fabricated diode, the oxidation process was quite simple, and the thickness of the grown oxide was easy to control (just by controlling the oxidation time and temperature), silicon dioxide was chosen to be the material for antireflective coating for the fabricated diode.

For SiO2:

Antireflection coating (SiO_2) $\rightarrow n_{SiO_2} = 1.46$

If the coating material was ideal, i.e. n =1.87, the thickness of the antireflection coating was calculated based on the following function:

$$d = m * \frac{\lambda}{4n} \quad \text{(eq1)}$$

where m = 1, 3, 5... is an odd integer

λ = the free-space wavelength

n = the refractive index of the coating material

Using this function (eq1), →

Thickness of SiO_2 -antireflection coating was:

For Red 632.8nm HeNe Laser -> d = 1084 A^0 or odd multiple of 1084 A^0 and

For Red 660nm LED -> d =1130 A^0 or odd multiple of 1130 A^0

However, silicon dioxide was not the ideal material for antireflective coating, an experiment was carried out to determine the optimal oxide thickness for antireflective coating. Five wafers were oxidized in air, at the same temperature of 1050 C. Every half hour of oxidation passed, one wafer was taken out of the furnace tube. These five wafers then went through couple reflection measurement methods as described in the "Test Measurement Methods".

III. Test Measurements Methods

1. Oxide thickness measurement method

An aluminum film was deposited on the oxidized wafers to form Metal Oxide Semiconductor (MOS) capacitors, which would be the necessary structure to be used to measure the grown oxide thickness using the capacitance-voltage method. Since the underlying semiconductor layer was N-type, positive biased DC voltage on the Al gate would attract the majority carrier electrons to the silicon surface. The capacitance measured therefore would be the oxide capacitance, Cox.

Measured capacitance = oxide capacitance per unit area, Cox

$$Cox = \frac{\epsilon A}{tox} = \frac{\epsilon_0 * \epsilon_{rSiO_2} * A}{tox}$$

where A = contact area of metal gate

tox = oxide thickness

When the gate biased voltage was negative, it would repel the majority carrier electrons from the surface creating a depleted region. As the biased voltage became

more negative, the depleted region would be larger. For larger values of negative DC gate voltage, the silicon surface would actually "invert" from N-type to P-type. The negative voltage on the gate would attract the minority carrier holes in the epi layer to the surface and if enough of them were present there, they could form an inversion layer of P-type carriers. The measured capacitance for negative voltage was the capacitance of the oxide and of the depletion layer. Since the depletion region with depended on the impurity concentration of the epi layer, a measurement of capacitance versus DC biased voltage could be used to extract the doping profile in the epi. The Mathematica file "tox and Nd calculation from C-V data.nb" showed the detail of this type of extraction.

If the interest was finding the thickness of the oxide, there only needed to apply positive biased DC voltage and measure the corresponding capacitance. The measured C-V data would be enough to calculate the oxide thickness.

2. Reflection measurement methods

The reflection measurement was carried out using two methods using two different light sources, i.e. a spot focused table lamp and 632.8nm HeNe laser. The first measurement method using the spot focused table lamp as the light source. Measurement instruments were the focused table lamp as the light source shining on reflecting surfaces, a spectrometer probe to detect the reflected light, a spectrometer to measure the intensity of the reflected light, an Ocean Optic. software and a computer to capture, store, and display the spectrum of the reflected light. It was important to mention that the intensity of the source was kept constant or assumed to be constant, and the probe was placed at the same distance and angle from reflected

surfaces for the purpose of consistency in the intensity measurement. Based on the measured intensity of the reflected light, reflectance of the oxide layers were determined.

The second method using 632.8nm HeNe as light source. The measurement set-up was shown in figure 5. Instruments were a 632.8nm HeNe as light source, a Radio Shack solar cell to capture the reflected light, a digital multimeter to measure the current generated by the solar cell. Since the solar cell would generate a larger current if it received more light, the surface that had the smallest solar cell current would be the surface that had smallest reflection, which was the best surface to be used as an antireflective coating for the fabricated diode.

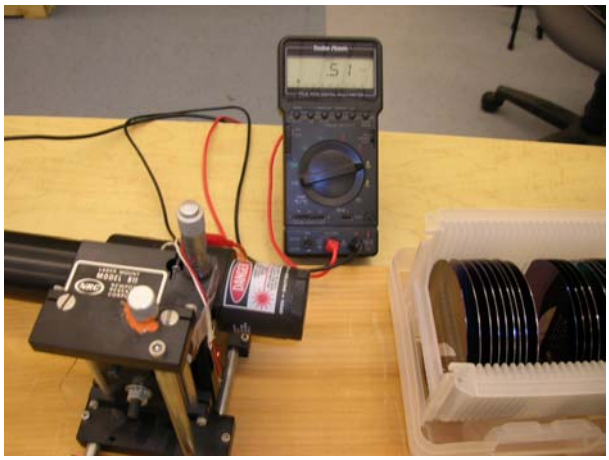


Figure 5: Set-up of the reflection measurement using a 632.8nm HeNe laser as light source.

3. Diode current measurement:

The diode current measured in this project was the short circuit current due to a large amount of leakage current generated by different imperfections in the fabrication. Digital multimeters were used to measure the voltage and current of the diode as well as the 660nm LED.

IV. Test Results:

A. Test Results from Experiments in Fabrication steps

Formula to calculate oxide thickness based on measured capacitance of the MOS capacitor (N type substrate) under forward bias.

$$\epsilon_{SiO_2} = 3.9;\ \epsilon_0 = 8.8542 * 10^{-12} (*\frac{F}{m}*);\ A = \pi \left(\frac{1.25\,mm}{2}\right)^2 = 0.01227 * 10^{-4} (*m^2*);$$

$$Cox = Cmeasured\ of\ positive\ Vbias\ (*F*);$$

$$tox = \frac{\epsilon_0 * \epsilon_{SiO_2} * A}{Cox}\ (*m*)$$

Wafer No.	Temperature (^{0}C)	Oxidation environment	Furnace Ramp up time (min)	Oxidation time (min)	Calculated oxide thickness (A^0)	Measured oxide thickness (A^0)	Measured C (pF) at Vbiased = + 10 Volts
1	1050	Air	90	30	655	810	523
2	1050	Air	90	60	953	1098	386
3	1050	Air	75	90	1200	1243	341
4	1050	Air	75	120	1417	1461	290
5	1050	Air	75	150	1611	1649	257

Table 2: Calculated and measured oxide thickness for 5 wafers in the antireflection coating experiment.

Note that the measured oxide thickness on all five test wafers were thicker than the calculated values from ~38 Angstroms to ~ 155 Angstroms. The furnace ramp up time when growing oxide on wafers #1 and #2 were 15 minutes longer than that when growing oxide on wafers #3, #4, and #5. And the data also showed that the oxide thickness on wafers #1 and #2 was consistently about 100 Angstroms thicker then that on wafer #3, #4 and #5. This indicated that some oxide was grown during the ramp up time at a temperature close to the oxidation temperature. Therefore, despite of the differences,

the measurement values of the oxide thickness on all five test wafers could reasonably be considered agreeing with the calculated values.

The following two plots were the plots of reflection and reflectance spectrum of reflected light from the experimental measured surfaces. Both plots showed that for red light having wavelength in ~ 650nm, the 1.461nm oxide layer, which was oxidized for two hours in air at 1050 C, was the best to be used as an antireflection coating for red light since its reflection or reflectance was the least. To make sure that this oxide layer was also the best when it was used as the antireflection coating for the 632.8nm HeNe laser, the reflection measurement using 632.8 nm HeNe laser as the light source. The data result and its plot shown in Table 3 and figure 8 also indicated that the same oxide layer thickness, i.e. 1.461nm oxide layer oxidized for two hours in air at 1050 C, was the best to be used as an antireflection coating for 632.8 nm HeNe laser. The results from the two measurement methods agreed with each other.

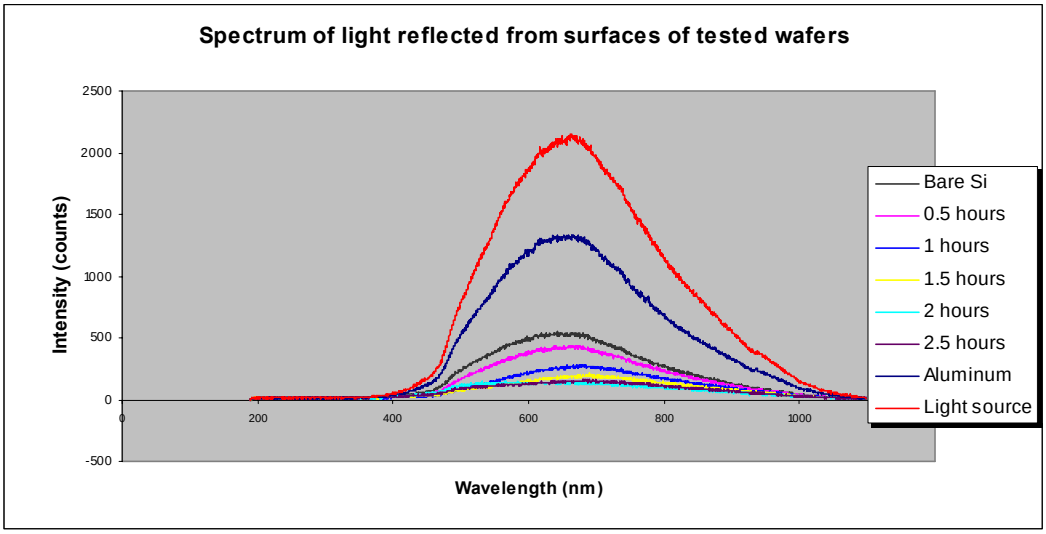


Figure 6: Reflection Spectrum of reflected light from experimental measurement surfaces.

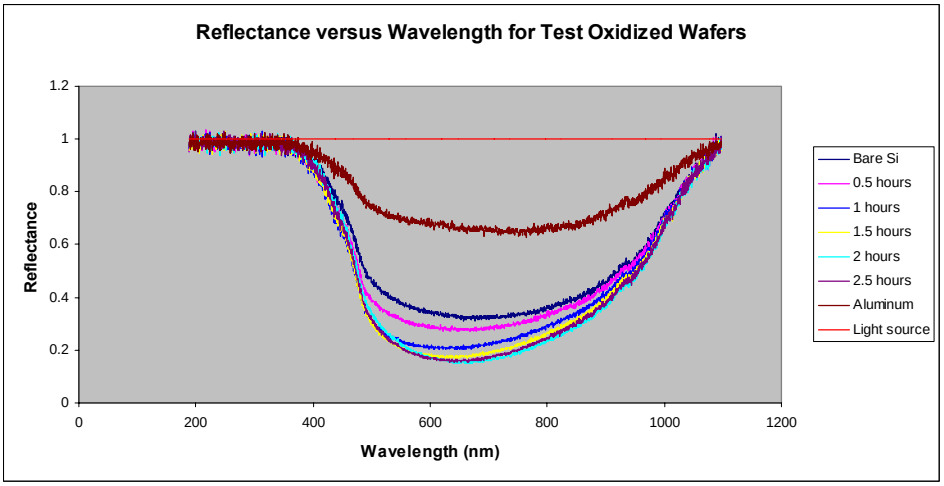


Figure 7: Reflectance Spectrum of reflected light from experimental measured surfaces.

Reflection from Red 632.8 nm HeNe Laser

I solar cell (Radio Shack) for back ground light in mA 0.05

Type	**Surfaces**	**I solar cell (mA) (Radio Shack)**	Adjusted I solar cell (mA)
1	Direct from light source	3.60	3.55
2	Aluminum	3.07	3.02
3	Bare silicon	1.26	1.21
4	Oxide thickness = 810 Angstroms	1.00	0.95
5	Oxide thickness = 1098 Angstroms	0.58	0.53
6	Oxide thickness = 1243 Angstroms	0.45	0.40
7	Oxide thickness = 1461 Angstroms	0.36	0.31
8	Oxide thickness = 1649 Angstroms	0.39	0.34

Table 3: Measured solar cell current for experimental reflected surfaces

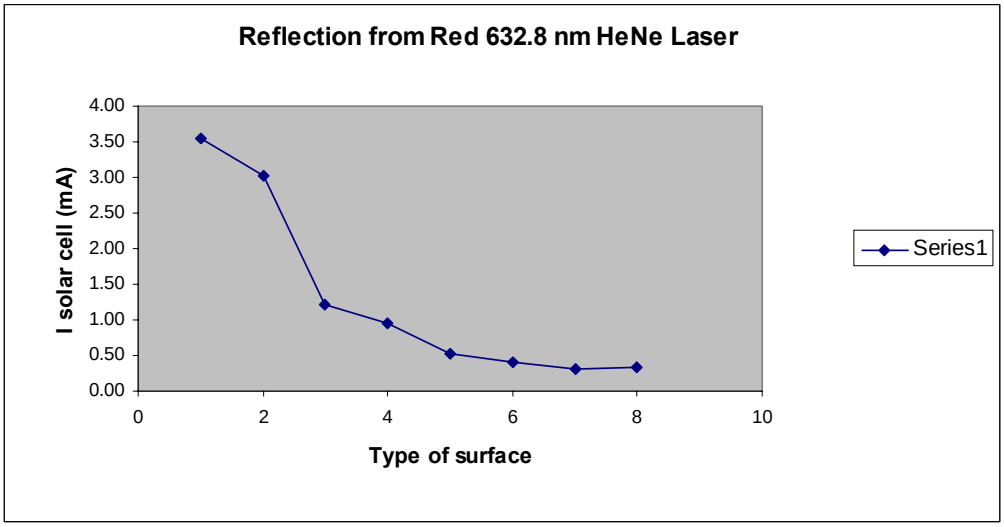


Figure 8: Plot of solar cell current versus reflected surfaces (data from table 3)

			Incident surfaces		Incident Oxide layer (thickness based on oxidation time of)				
	Wavelength (nm)	Light source	Al	Barer Si	30 min (0.810 nm)	60 min (1.098 nm)	90 min (1.243 nm)	120 min (1.461 nm)	150 min (1.649 nm)
HeNe Laser	632	2268	1502	749	639	483	395	362	374
	Intensity (counts) Ajusted for background light ------->	2040	1274	521	411	255	167	134	146
	% Reflection	100.00%	62.45%	25.54%	20.15%	12.50%	8.19%	6.57%	7.16%
	% improvement compared to bare Si surface			0.00%	21.11%	51.06%	67.95%	74.28%	71.98%
Red LED	660	2337	1544	750	654	490	408	356	381
	Intensity (counts) Ajusted for background light ------->	2109	1316	522	426	262	180	128	153
	% Reflection	100.00%	62.40%	24.75%	20.20%	12.42%	8.53%	6.07%	7.25%
	% improvement compared to bare Si surface			0.00%	18.39%	49.81%	65.52%	75.48%	70.69%

Table 4: Reflection data for experimental measured surfaces.

It was the fact that the bare silicon surface would reflect 31 % of incident light. The results shown in table 4 suggested that with an oxide antireflection coating, the reflection reduced. And for the case when the best 1.461nm oxide antireflection coating was applied on the silicon surface, the reflection would be improved by ~75 %.

B. Test Results for I-V characteristics of P-N junction

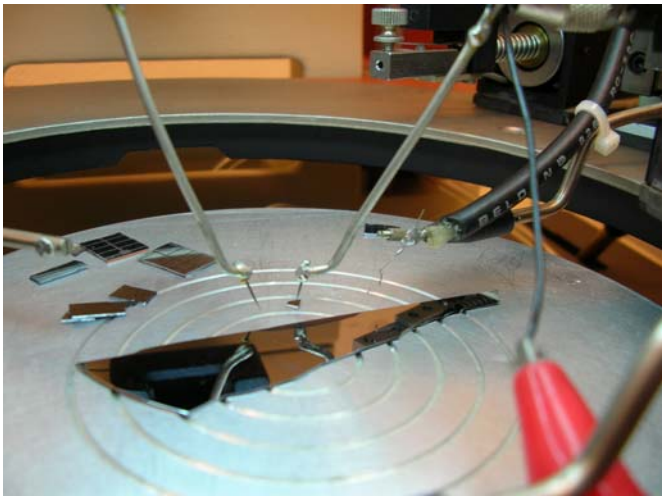
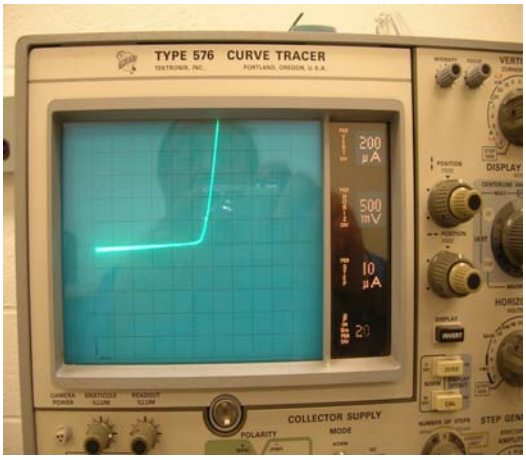
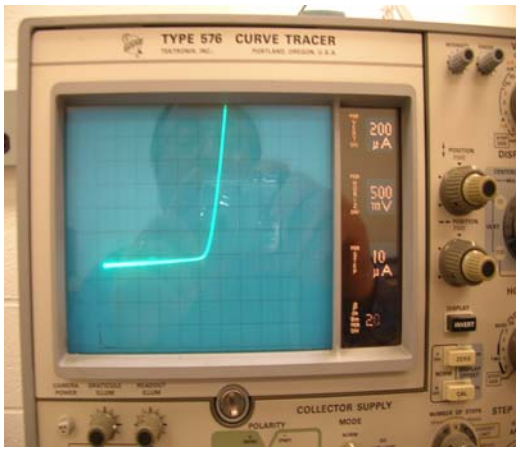


Figure 9: Tested sample (25 min. B diffusion at 1050^0C in N2)
Calculated junction depth, Xj = 0.82 micron



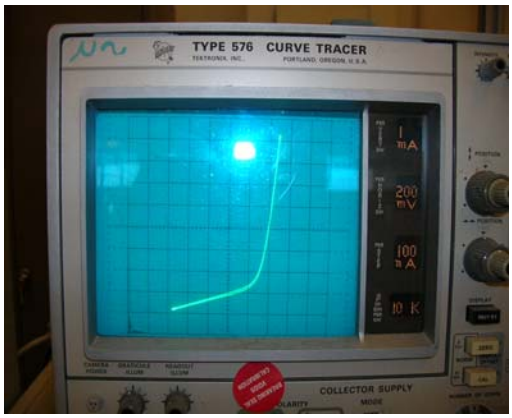


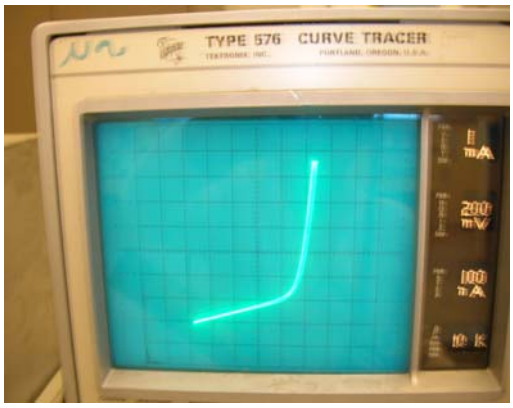
I-V diode - no light I-V diode - working light

Figure 10: I-V characteristics of P-N junction without and with incident light.

The pictures shown in figure 10 were the I-V plots of the tested diode under no illumination and with illumination. When the tested diode was illuminated with a working light, the curve on the left picture shifted down indicated a larger current was generated. This meant that there existed a p-n junction, which was the core of the diode. Therefore, a working diode had been fabricated.

Tests were carried out on another sample from the same processed wafer as the previous sample using 632.8nm HeNe laser and red 660nm LED as incident light sources





I-V Diode in responding to Red 660nm LED light

I-V Diode in responding to Red 632.8nm HeNe Laser beam

Figure 11: I-V curves of the fabricated diode when it was illuminated with red 660 nm LED and 632.8 nm HeNe laser beam.

Information about the red LED used in the tested I-V measurement:

Wavelength Red LED = 660 nm

I LED = 20mA, (max = 50mA)

Power dissipation = max = 100mW

Vin (V)	VR(V) R= 85.3Ω	I_{LED} (mA)	V_{LED} (V)	P_{LED} (mW)	Idiode (mA)	Vdiode (V)	Pdiode (mW)	Isolar cell (mA)	Vsolar cell (mV)	Psolar cell (mW)	(Pdiode/ Psolar cell)
3.200	1.706	20.000	1.494	29.880	1.310	357.400	0.468	1.590	356.700	0.567	0.826
3.600	2.133	25.000	1.468	36.690	1.650	371.800	0.613	2.080	375.400	0.781	0.786
4.100	2.559	30.000	1.541	46.230	1.970	382.000	0.753	2.470	390.300	0.964	0.781
4.500	2.986	35.000	1.515	53.010	2.330	390.000	0.909	2.850	402.000	1.146	0.793
5.000	3.412	40.000	1.588	63.520	2.660	398.000	1.059	3.250	410.000	1.333	0.795
5.400	3.839	45.000	1.562	70.270	2.900	402.000	1.166	3.600	419.000	1.508	0.773
5.800	4.265	50.000	1.535	76.750	3.210	407.000	1.306	3.990	425.000	1.696	0.770

Table 5: Voltage, current, and power of 660nm LED and solar cell

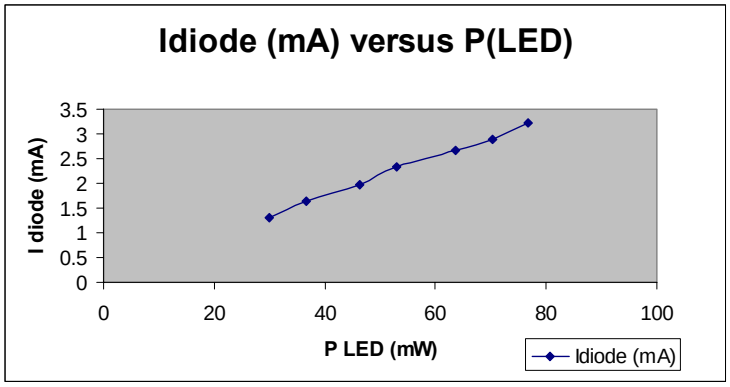


Figure 12: Plot of current of fabricated diode versus power of 660nm LED

The plot of I diode versus P LED showed that the Idiode increased as the power of the LED, PLED, increased. This was expected for a working diode.

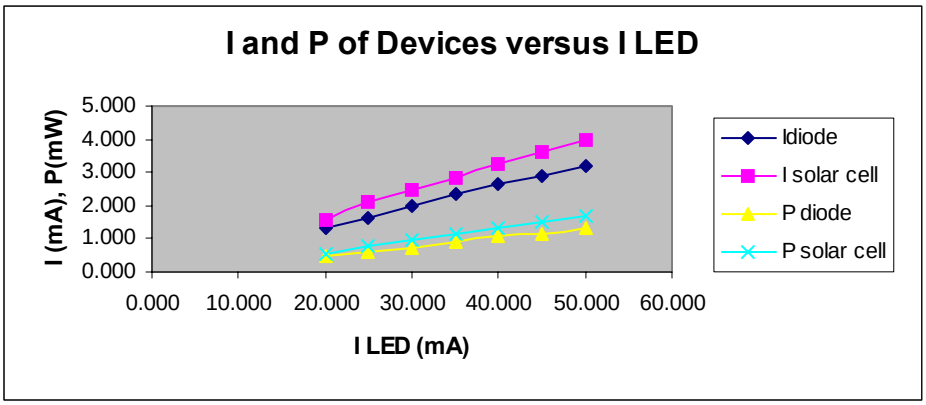


Figure 13: Plot of current and power of fabricated diode and solar cell (for comparison) versus current of 660nm LED

The plot in figure 13 was just for the comparison between I and P of the fabricated diode and the Radio Shack solar cell. Based on the information shown in table 5, the power generated by the fabricated diode was about 80% compared to that of the solar cell. Due to many fabrication equipment's constrains, the result diode wasn't too bad comparing to the commercial Radio Shack solar cell.

Efficiency:

Theoretical photocurrent generated was:

$Iph = R * P_0$

Where • Iph is photocurrent (A)

- R is radiant sensitivity or spectral responsivity (A/W)
- P_0 is optical power (W)

Since the surface of the tested p-n junction diode was bare silicon (without antireflection coating), and it was the fact that 31% of incident light reflected from the silicon surface, the efficiency of the diode was calculated with an assumption that only 70 percent of the 660nm LED optical power would be considered as the optical power received by the diode. So,

P reflection = 30% P(LED) → Po =(1-0.3) P(LED) = 0.7 P(LED)

Iph =R * Po = 0.4 * Po

Efficiency = (Idiode/ Iph) *100%

R = ~0.4 A/W for wavelength of 600nm-> 650nm

V_{LED}(V)	I_{LED}(mA)	P_{LED}(mW)	Idiode (mA)	Iph(mA)	Efficiency
1.494	20	29.88	1.31	8.3664	15.65787
1.468	25	36.69	1.65	10.2732	16.06121
1.541	30	46.23	1.97	12.9444	15.21894
1.515	35	53.01	2.33	14.8428	15.69785
1.588	40	63.52	2.66	17.7856	14.95592
1.562	45	70.27	2.9	19.6756	14.73907
1.535	50	76.75	3.21	21.49	14.93718

Table 6: V, I, and P of 660nm LED and Idiode, Iph, and Efficiency of the fabricated photodiode

Data from table 6 showed that the fabricated diode had an efficiency of ~ 15 %. The highest efficiency of the diode was 16% when the LED was operated at 25 mA.

V. Conclusion

Even though the fabricated diode wasn't a desire photodiode, it response to red 660nm LED and 632.8nm HeNe laser as intended. The short circuit current generated by the diode was ~ 2 mA when the HeNe laser beam illuminated it. For the LED case, the short circuit current varied depending on the operating current of the LED, which was equivalent to the optical power of the LED. The highest efficiency of the diode was 16% when the LED was operated at 25 mA. For the antireflection coating, although the reflective coating wasn't applied on the fabricated diode before the final test measurements were carried out, the experiments on the oxidation and antireflection coating had been done, and the results for the experiment had been obtained. Anyway, a working photodiode was fabricated.

VI. Appendixes

- Mathematica files (4 files):
    1. "Calculations for fabrication parameters.nb"
    2. "tox and Nd calculation from C-V data.nb"
    3. "tox calculation from C-V data for 5 wafers.nb"
    4. "Reflection of oxide layers (measured, using a focused table lamp).nb"
- Excel files (4 files):
    1. "Collected C-V from test wafer and C-V plots.xls"
    2. "Data and spectrum of reflected light.xls"
    3. "Reflection from HeNe Laser (measured).xls"
    4. "I-I,P diode and solar cell and power efficiency.xls"

VII. References

1. Kasap, S.O., Optoelectronics and Photonics, Prentice Hall, 2001.
2. Jaeger, Richard C., Introduction to Microelectronic Fabrication, 2nd ed., Vol. V, Prentice Hall, 2002.
3. Plummer, James D., Deal, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Prentice Hall, 2000.
4. "Photodiode Characteristics and Applications", UDT Sensors Inc., http://www.udt.com
5. "Silicon Photodiodes: Physics and Technology", UDT Sensors Inc., http://www.udt.com
6. Green, M. A., Solar Cell, Prentice- Hall, 1982
7. Kasap, S.O., Principles of Electronic Materials and Devices, 2nd ed., McGraw-Hill, 2002.

Equipments used in the test measurement in this project

- Signatone (CA) S-1041 HC Serial 132
- Boonton Electronics, Digital Capacitance Meter 72BD
- DC Regulated Power Supply (China) CSI30003X III
- Type 576 Curve Tracer (Oregon, USA), Textronix
- High-Resolution Spectrometer, Ocean Optics, HR 2000CG-UV-NIR
- Leica Focus Light
- Digital Multimeter