Summary
of

# MUMPS

# A 3-LAYER POLYSILICON SURFACE MICROMACHINING PROCESS

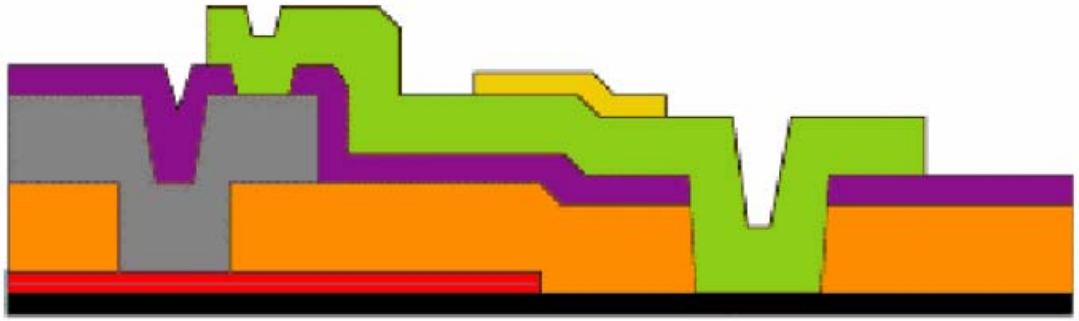

**FIGURE 1.1.** Cross sectional view showing all 7 layers of the PolyMUMPs process (not to scale).

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Poly0 | | Poly1 | | Poly2 | | Metal |
| | Nitride | | 1st Oxide | | 2nd Oxide | | |

Figure 1.1 is a cross section of the three-layer polysilicon surface micromachining PolyMUMPs process. This process has the general features of a standard surface micromachining process: (1) polysilicon is used as the structural material, (2) deposited oxide (PSG) is used as the sacrificial layer, and silicon nitride is used as electrical isolation between the polysilicon and the substrate. The process is different from most customized surface micromachining processes in that it is designed to be as general as possible, and to be capable of supporting many different designs on a single silicon wafer. Since the process was not optimized with the purpose of fabricating any one specific device, the thicknesses of the structural and sacrificial layers were chosen to suit most users, and the layout design rules were chosen conservatively to guarantee the highest yield possible.


**FIGURE 1.2.** The surface of the starting n-type (100) wafers are heavily doped with phosphorus in a standard diffusion furnace using POCl 3 as the dopant source. A 600 nm blanket layer of low stress silicon nitride (Nitride) is deposited followed by a blanket layer of 500 nm polysilicon (Poly 0). The wafers are then coated with UV-sensitive photoresist.

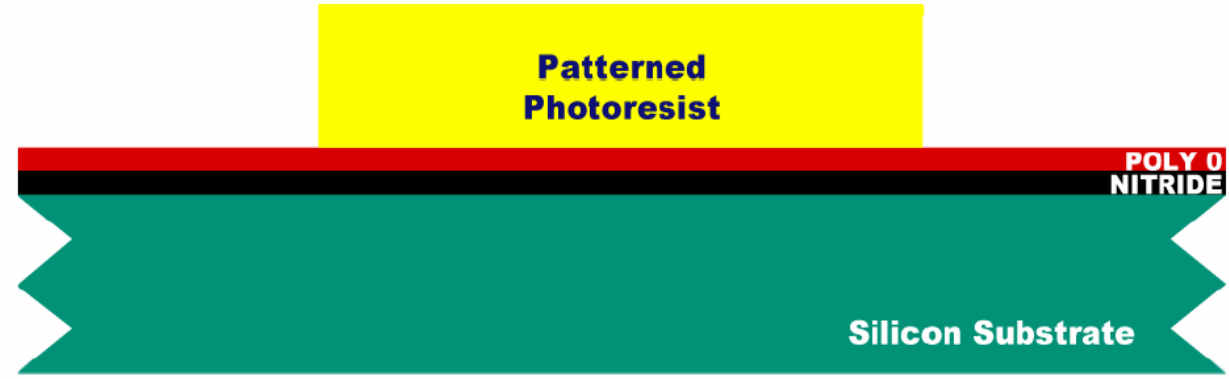


**FIGURE 1.3.** The photoresist is lithographically patterned by exposing it to UV light through the first level mask (POLY0) and then developing it. The photoresist in exposed areas is removed leaving behind a patterned photoresist mask for etching.

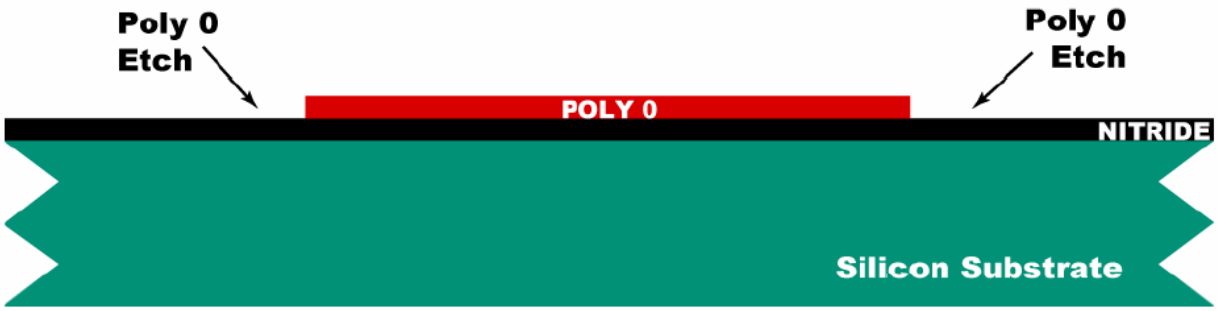


**FIGURE 1.4.** Reactive ion etching (RIE) is used to remove the unwanted polysilicon. After the etch, the photoresist is chemically stripped in a solvent bath. This method of patterning the wafers with photoresist, etching and stripping the remaining photoresist is used repeatedly in the PolyMUMPs process.


**FIGURE 1.5.** A 2.0 μm layer of PSG is deposited on the wafers by low pressure chemical vapor deposition (LPCVD). This is the first sacrificial layer.


**FIGURE 1.6.** The wafers are coated with photoresist and the second level (DIMPLE) is lithographically patterned. The dimples, 750 nm deep, are reactive ion etched into the first oxide layer. After the etch, the photoresist is stripped.

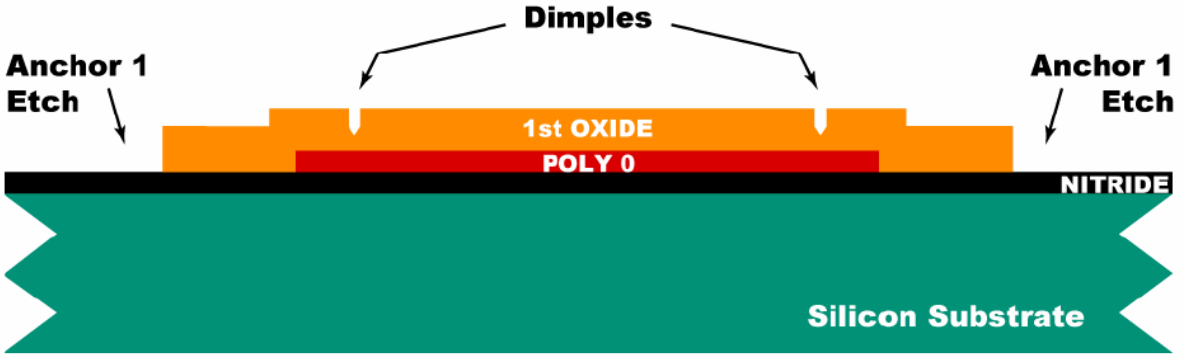


**FIGURE 1.7**. The wafers are re-coated with photoresist and the third level (ANCHOR1) is lithographically patterned. The unwanted oxide is removed in an RIE etch and the photoresist is stripped.

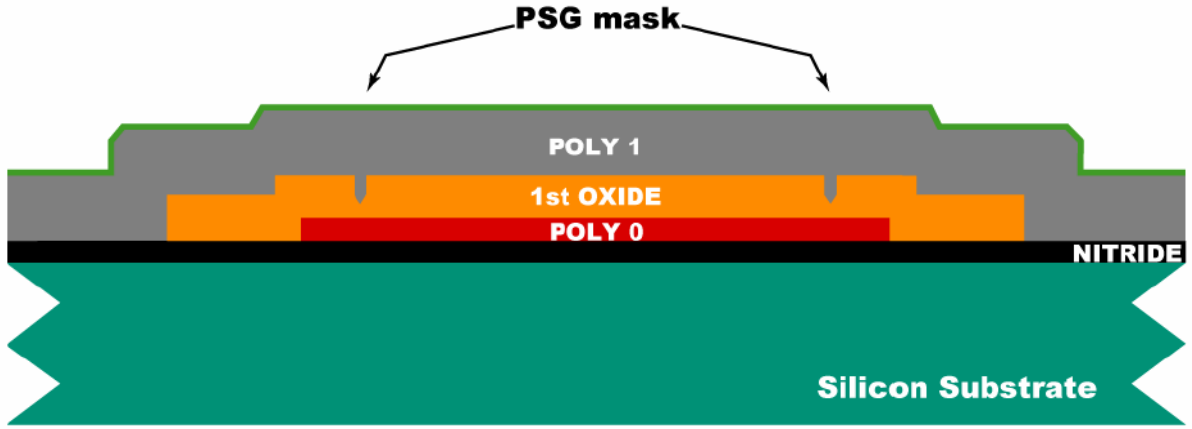


**FIGURE 1.8.** A blanket 2.0 μm layer of un-doped polysilicon is deposited by LPCVD followed by the deposition of 200 nm PSG and a 1050°C/1 hour anneal. The anneal serves to both dope the polysilicon and reduce its residual stress.


**FIGURE 1.9.** The wafer is coated with photoresist and the fourth level (POLY1) is lithographically patterned. The PSG is first etched to create a hard mask and then Poly 1 is etched by RIE. After the etch is completed, the photoresist and PSG hard mask are removed.

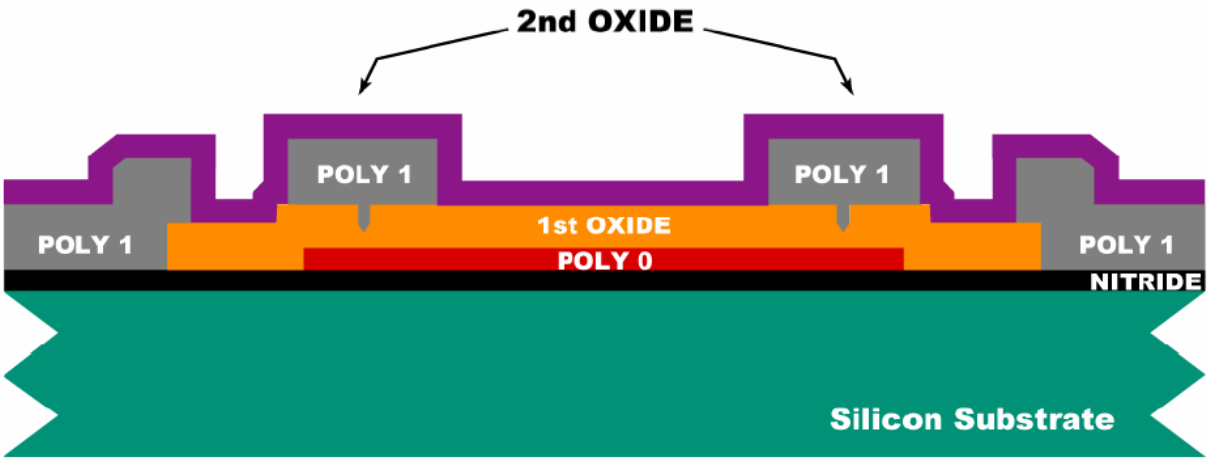


**FIGURE 1.10.** The Second Oxide layer, 0.75 μm of PSG, is deposited on the wafer. This layer is patterned twice to allow contact to both Poly 1 and substrate layers.

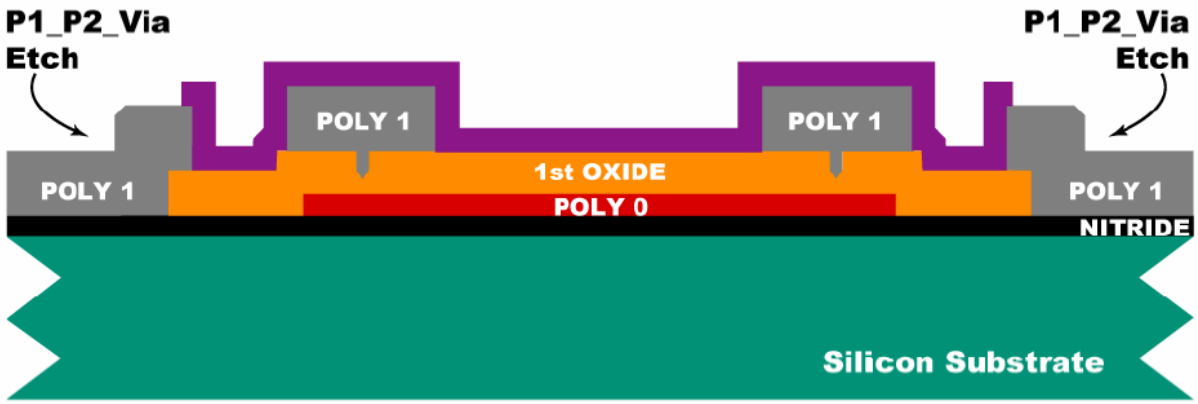


**FIGURE 1.11**. The wafer is coated with photoresist and the fifth level (POLY1_POLY2_VIA) is lithographically patterned. The unwanted Second Oxide is RIE etched, stopping on Poly 1, and the photoresist is stripped.

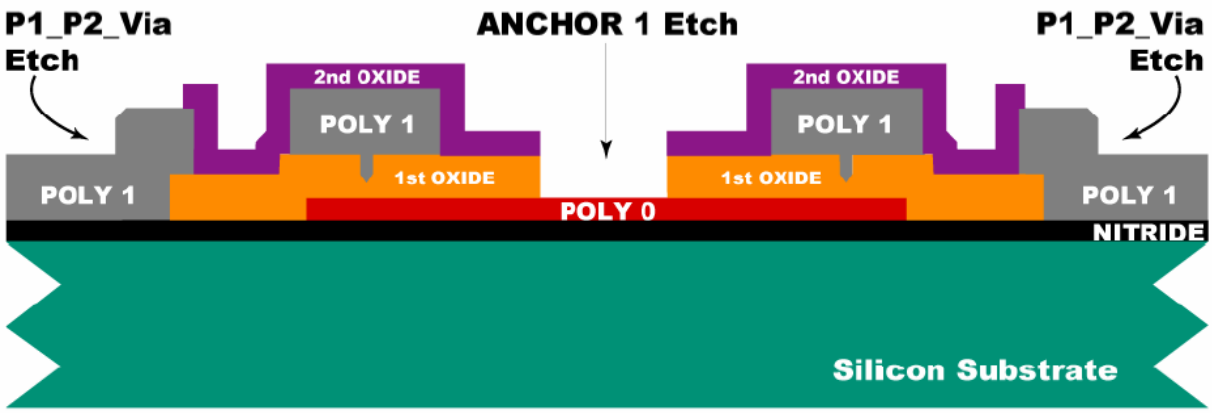


**FIGURE 1.12**. The wafer is re-coated with photoresist and the sixth level (ANCHOR2) is lithographically patterned. The Second and First Oxides are RIE etched, stopping on either Nitride or Poly 0, and the photoresist is stripped. The ANCHOR2 level provides openings for Poly 2 to contact with Nitride or Poly 0.

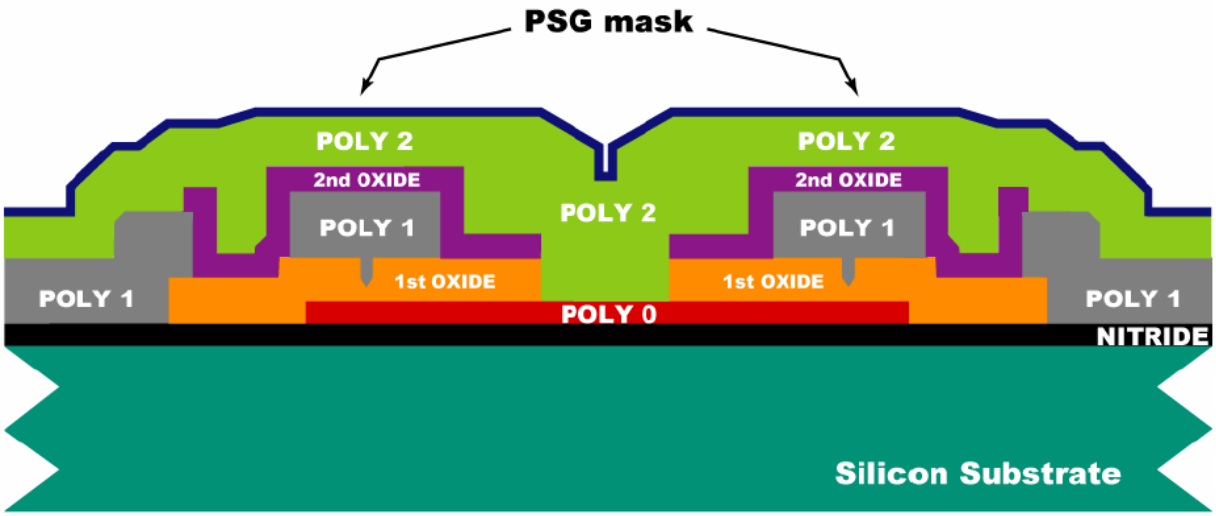


**FIGURE 1.13.** A 1.5 μm un-doped polysilicon layer is deposited followed by a 200 nm PSG hardmask layer. The wafers are annealed at 1050°C for one hour to dope the polysilicon and reduce residual stress.

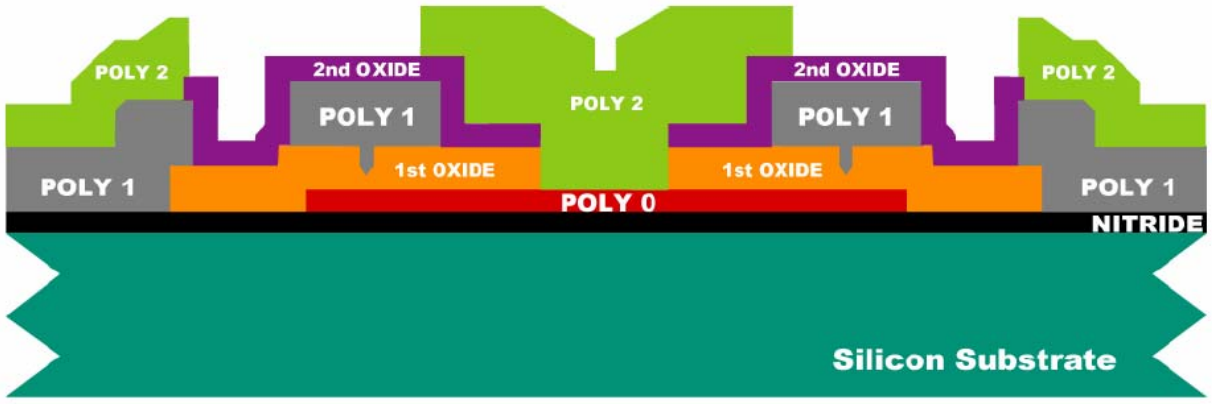


**FIGURE 1.14.** The wafer is coated with photoresist and the seventh level (POLY2) is lithographically patterned. The PSG hard mask and Poly 2 layers are RIE etched and the photoresist and hard mask are removed. All mechanical structures have now been fabricated. The remaining steps are to deposit the metal layer and remove the sacrificial oxides.

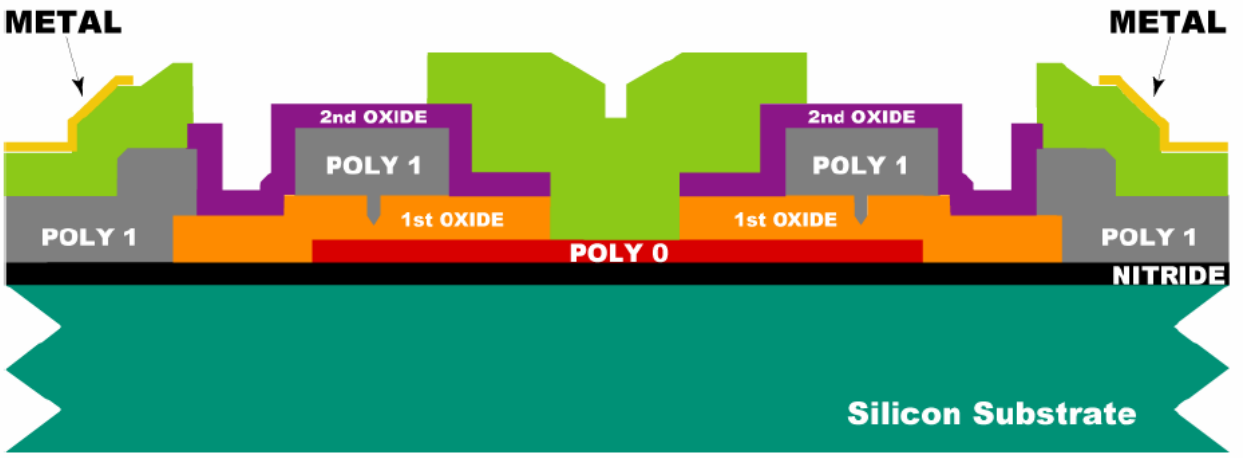


**FIGURE 1.15.** The wafer is coated with photoresist and the eighth level (METAL) is lithographically patterned. The metal (gold with a thin adhesion layer) is deposited by lift-off patterning which does not require etching. The side wall of the photoresist is sloped at a reentrant angle, which allows the metal to be deposited on the surfaces of the wafer and the photoresist, but provides breaks in the continuity of the metal over the reentrant photoresist step. The photoresist and unwanted metal (atop the photoresist) are then removed in a solvent bath. The process is now complete and the wafers can be coated with a protective layer of photoresist and diced. The chips are sorted and shipped.

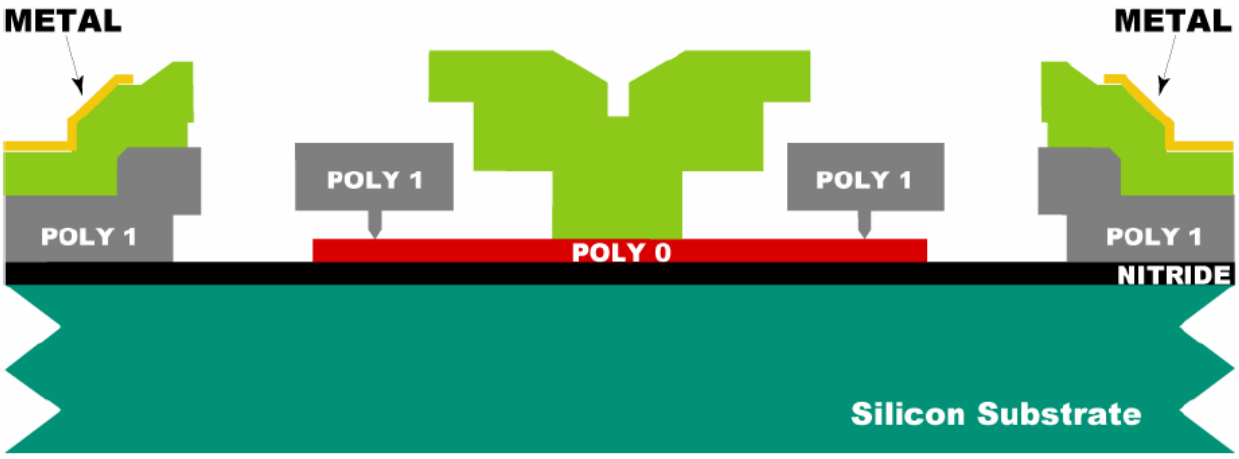


**FIGURE 1.16.** The structures are released by immersing the chips in a 49% HF solution. The Poly 1 "rotor" can be seen around the fixed Poly 2 hub. The stacks of Poly 1, Poly 2 and Metal on the sides represent the stators used to drive the motor electrostatically.

| Material Layer | Thickness (μm) | Lithography Level Name |
|---|---|---|
| Nitride | 0.6 | -- |
| Poly 0 | 0.5 | POLY0 (HOLE0) |
| First Oxide | 2.0 | DIMPLE<br>ANCHOR1 |
| Poly 1 | 2.0 | POLY1 (HOLE1) |
| Second Oxide | 0.75 | POLY1_POLY2_VIA<br>ANCHOR2 |
| Poly 2 | 1.5 | POLY2 (HOLE2) |
| Metal | 0.5 | METAL (HOLEM) |

**TABLE 2.1**. Layer names, thicknesses and lithography levels. Hole levels are printed on the same line as their corresponding polysilicon or metal levels.

Source: PolyMUMPS DESIGN HANDBOOK Rev. 8.0