Figure 1. Common-Source N-Channel JFET Small-Signal AC Amplifier

Figure 2. Midrange SSAC Equivalent of The Common-Source JFET Amplifier
- **Input and Output Impedances:**

\[
R_{in} = \frac{V_{in}}{I_{in}} = R_G \quad R_{in} = R_G \quad R_{out} = r_{ds} \parallel R_D
\]

- **Voltage Gain, \( A_v \):**

\[
A_{VO} = \left( \frac{V_{out}}{V_{in}} \right)_{RL=\infty} = \frac{-g_m \Delta V_{GS} (r_{ds} \parallel R_D)}{\Delta V_{GS}}
\]

\[
A_{VO} = -g_m (r_{ds} \parallel R_D) = -g_m R_{out}
\]

- **DC ANALYSIS**

![DC Equivalent Circuit](image)

Figure 3. DC Equivalent of The Common-Source N-Channel JFET Amplifier
Graphical Analysis

Figure 4. The Common-Source JFET Amplifier: Graphical Analysis of its Q-Point

- JFET is operated in saturation.

1. \[ I_{DQ} = I_{DSS} \left( 1 - \frac{V_{GSQ}}{V_{PC}} \right)^2 (1 + \lambda V_{DSQ}) \]

   Loop I: \[ V_{GSQ} = (V_{GG} - R_G I_{GQ}) - (R_s I_{DQ}) \]
   
   \( R_s I_{GQ} \) is negligible since gate is reverse biased.

2. \[ V_{GSQ} = V_{GG} - R_s I_{DQ} \]
   Null

Note that for N-channel JFET, \( V_{GG} > V_{GSQ} \), and therefore \( V_{GG} \) can be assigned negative, zero, or positive values since \( V_{GSQ} \) is negative.

Positive values of \( V_{GG} \) are preferred since they can be obtained by employing a simple voltage divider from the \( V_{DD} \) source, making operation with only one power supply possible.

A more attractive case is \( (V_{GG} = 0) \) which does not require a \( V_{GG} \) supply at all. This latter case is popular among designers and is referred to as THE SELF-BIASED JFET amplifier.
- Example: Design an N-Channel JFET Common-Source SS amplifier which operates from a single power supply and delivers

\[
A_{VO} = 20 \quad f_{-3\,dB} \leq 50 \, Hz \\
R_{out} = 20 \, K\Omega \quad R_{in} = 470 \, K\Omega \quad R_G = R_{in} = 470 \, K\Omega \quad R_{out} = 20 \, K\Omega \, m\Omega = r_{ds} \# R_D
\]

JFET parameters: \( I_{DSS} = 5 \, mA \quad V_{PO} = -3 \, V \quad \lambda = 0.02 \)

\[ |A_{VO}| = g_m \, R_{out} \quad \implies \quad g_m = \frac{A_{VO}}{R_{out}} = \frac{20}{20 \, K} = 0.001 \, S = 1 \, mS \]

Pick \( V_{DSQ} = 5 \, V \)

\[ g_m = 2 \, \frac{I_{DSS}}{(-V_{PO})} \left( 1 - \frac{V_{GSQ}}{V_{PO}} \right) (1 + \lambda \, V_{DSQ}) \]

\[ 0.001 = \frac{2 \times 5 \, mA}{3} \left( 1 - \frac{V_{GSQ}}{V_{PO}} \right) (1 + 0.02 \times 5) \]

\[ x = \left( 1 - \frac{V_{GSQ}}{V_{PO}} \right) = \frac{3}{2 \times 5 \times 1.1} = 0.273 \]

\[ V_{GSQ} = V_{PO} (1 - x) = -3 \, (0.727) = -2.18 \, Volts \, DC \]

\[ I_{DQ} = I_{DSS} \, (x)^2 \ (1 + \lambda \, V_{DSQ}) = 5 \, mA \ (0.273)^2 \, 1.1 = 0.41 \, mA \]
Figure 5. JFET Amplifier Bias Circuit (Example)

\[ V_{GSQ} = V_{GG} - R_G I_{GQ} - R_s I_{DQ} \]
\[ V_{GSQ} = -R_s I_{DQ} \rightarrow R_s = \frac{-V_{GSQ}}{I_{DQ}} = \frac{2.18}{0.41 \text{ mA}} \]
\[ R_s = 5.3 \text{ K}\Omega \]

\[ \text{R}_{\text{out}} = r_{ds} \parallel R_D = 20 \text{ K}\Omega \]

\[ g_{ds} = \frac{I_{DQ}}{1/\lambda + V_{DSQ}} = \frac{0.41 \text{ mA}}{50 + 5} = \frac{1}{134 \text{ K}\Omega} \]

\[ 20 \text{ K}\Omega = R_D \parallel (134 \text{ K}\Omega) \rightarrow R_D = 23.5 \text{ K}\Omega \]

\[ V_{DD} = R_D I_{DQ} + V_{DSQ} + R_s I_{DQ} \]
\[ V_{DD} = 23.5 \times 0.41 + 5 + 2.18 \]
\[ V_{DD} = 16.8 \text{ V DC} \]

Note that this calculated value of \( V_{DD} \) is not a standard value. The engineer has to pick a standard value greater than this, like 18 VDC. In that case the excess voltage 18 - 16.8 = 1.2 V will add to the JFET's \( V_{DSQ} = 5 + 1.2 = 6.2 \text{ V} \), resulting in a need for reiteration of the calculations given above.
Small values of $\lambda$, through which $V_{DSQ}$ affects the design calculations, assures no more than one iteration to be sufficient for a self-consistent result.