1. Operational Amplifier Design: (70 pts)

\[ V_{TON} = -V_{TOP} = 1V, \quad K_{PP} (PMOS) = 20 \text{ uA/V}^2, \quad K_{PN} (NMOS) = 50 \text{ uA/V}^2, \quad \lambda_N = 0.01, \quad \lambda_P = 0.03, \quad \gamma_N = \gamma_P = 0 \]

\[ C_{OX} = 0.004 \text{ F/m}^2, \quad C_{OX_{poly1-poly2}} = 0.002 \text{ F/m}^2 \]

Take \( L = 4\text{um for all transistors} \) \( VDD = 5\text{VDC}, \quad VSS = -5\text{VDC}, \quad RL = 10K, \quad CL = 200pF, \quad GBW = 3141\text{Krad/s}, \quad Av = 50,000 \)

1a. Draw the circuit diagram of the operational amplifier you have designed for your class project. Label all transistors as M1, M2, etc. Use 4-terminal symbol transistors to clearly show the type as well as all four connections of it in the circuit. Indicate, with constant current source symbols which transistors are not involved in signal amplification (the d.c. biasing transistors).

(No partial credits will be given for incomplete or malfunctional circuits!) (15 pts)
1b. Design the output stage for an output swing of +/- 3Vpeak at a slew rate of 1 V/us.  
   (Calculate the bias current and W/L ratio of the active transistor.) (12 pts)

1c. Calculate the compensation capacitance needed for a "good" (i.e. ~60 degrees) phase margin. (7 pts)
Assume $CC = 2pF$ was calculated in 1.c. Design the first stage, i.e. calculate the operating point currents and $W/L$ of its active transistors to satisfy the slew rate and gain bandwidth product. (Do not calculate $W/L$ of the active load transistors, yet.) (12 pts)
1e. Assuming the second stage has to satisfy $\frac{gm}{Cc} = 2.2 \text{ GBW}$ and your first stage delivers a gain of 500, design the second stage (i.e. calculate $W/L$ and operating current of its transistors) to make up for the total gain specified. (12 pts)

1f. Assume the reference current, and the first, second and third stage bias currents to have been calculated to be 10uA, 1uA, 2uA and 120uA, respectively, and $(W/L)$s of 2nd stage active transistor and the reference transistor to be 20/1, calculate $(W/L)$s of the rest of the transistors in the circuit. (12 pts)
2. Layout: (15 pts.)

Draw the cross sections and layout diagrams (*indicate dimensions*) of,

a. a 2 pF Cc capacitor

b. W=10 um L=4 um PMOS
3. Current/Voltage References: (20 pts.)

a. Draw the circuit diagram of a CASCODED Current Mirror.
b. Use small signal analysis to prove that its output resistance is significantly higher than ordinary current mirror.