1.a. What properties of Silicon make it better suited for integrated circuit fabrication compared to GaAs? Give a list and explain why?

1.b. Briefly describe the “LOCOS” process. What is “Bird’s Beak”? What materials/chemicals are essential to do LOCOS? Why do you need a “recessed” structure?
1. c. Compare “Ion Implantation” with “Diffusion” for selective doping of Silicon.

2. Give the cross-sectional structures and top view patterns of junctions/layers of the following devices which were fabricated in a standard bipolar process.

   a. NPN  
   b. Lateral PNP  
   c. Pinch Resistor
4. CMOS Process:

a. With the help of cross sectional drawings on the left side of the page and top view drawings on the right describe all the steps of fabrication of a CMOS inverter cell in an P-Well CMOS Process. Identify (without skipping) every masking layer up to and including METAL1.

b. On the final step mark the length (L) and the width (W) of the resulting MOSFETs with arrows.

c. If NEGATIVE photoresist is being used throughout the process redraw your POLY and METAL1 mask patterns and cross hatch the areas that need to be dark on the mask.

<table>
<thead>
<tr>
<th>CROSS SECTION</th>
<th>TOP VIEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>NMOS</td>
</tr>
</tbody>
</table>
**Diffusion/Oxidation Data for Problem 5:**

<table>
<thead>
<tr>
<th></th>
<th>D@1000C</th>
<th>D@1100C</th>
<th>Solubility@1000</th>
<th>Solubility@1100</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Boron</strong></td>
<td>3.0E-15 cm²/s</td>
<td>2.0E-14 cm²/s</td>
<td>2.0E20 cm⁻³</td>
<td>3.0E20 cm⁻³</td>
</tr>
<tr>
<td><strong>Phosphorus</strong></td>
<td>4.0E-15 cm²/s</td>
<td>3.0E-14 cm²/s</td>
<td>8.0E20 cm⁻³</td>
<td>1.2E21 cm⁻³</td>
</tr>
</tbody>
</table>

Hole mobility (average): 250 cm²/V.s  
Electron mobility (average): 1000 cm²/V.s

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5. 1E17 /cm³ uniformly doped P-type Silicon substrates are being used to make P-N junction diodes. In the process a **pre-deposition** step at 1000 C for 1 hour is being followed by a **drive-in diffusion** of 3 hours at 1100 C.

Find:

a. the surface concentration after the predep,
b. the minimum oxide thickness for masking and the color of the oxide,
c. the surface concentration after drive in, N(0),
d. the final junction depth, xj,
e. the final sheet resistance of the diffused layer, Rs.
1. Assume a square shaped wafer of 200 mm x 200 mm size undergoes an IC process which results in 100 point defects uniformly distributed on it at the end. Determine, for each case below, how many good die and how much die yield this wafer/process combination would produce.

<table>
<thead>
<tr>
<th>Die size</th>
<th>Total Die</th>
<th>Good Die</th>
<th>Die Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. 20 mm x 20 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b. 5 mm x 5 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>c. 1 mm x 1 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
1. Assume a square wafer of 10 cm x 10 cm size undergoes an IC process which results in 100 point defects uniformly distributed on it at the end. Determine, for each case below, how many good die and how much die yield this wafer/process combination would produce.

<table>
<thead>
<tr>
<th>Die size</th>
<th>Total Dice</th>
<th>Good Dice</th>
<th>Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. 2 cm x 2 cm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b. 1 cm x 1 cm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>c. 0.5 cm x 0.5 cm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>d. 1 mm x 1 mm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2. a. What properties of Silicon make it better suited for integrated circuit fabrication compared to GaAs? Why?
   b. Where does GaAs have advantage over Silicon? Why?

3. What is the meaning of "segregation coefficient"? Explain its effect on the Czochralski growth of Silicon.

   What happens to the crystal grown if the segregation coefficient is
   a. < 1
   b. = 1
   c. < 1 ?

4. Draw a unit cube representing a cubic crystal. Indicate the axes on it.
   a. Show (010), 110 and (113) planes on it.

5. (10% Bonus) How would you kill the rectifying properties of Schottky barriers formed between Silicon and Aluminum in an integrated circuit? Explain briefly the tricks used.
1. A boron predeposition at 1100 C gives a dopant dose \( Q \) of \( 1 \times 10^6 \) cm\(^{-2}\). It is followed by a drive-in diffusion of one hour at 1000 C. Find:
   a. the surface concentration after the predep,
   b. the time it took for the predeposition,
   c. the surface concentration after drive in, \( N(0) \), and
   d. the junction depth after all of these steps if the wafer was initially doped with phosphorous at \( 1 \times 10^5 \) level.
   e. What if the initial doping was boron at \( 1 \times 10^5 \) in (d)?

2. Briefly describe,
   a. What is Solid Solubility?, Where does it apply in device/wafer fabrication?
   b. What is equilibrium and non-equilibrium process? Describe what makes the two different and give examples for an equilibrium and for a non-equilibrium doping process.
   c. It was shown in class that sheet resistance of a doped layer independent of doping profile. What is the assumption leading to that conclusion?

\[
R_{\text{sheet}} = \frac{1}{(q \cdot \mu \cdot Q)}
\]

3. A P-type doped wafer (\( 1 \times 10^6 \)) and 1100 C 1Hr phosphorous diffusion is being used to make silicon N+P diodes.
   a. What is the junction depth?
   b. What is the oxide thickness needed to do an effective mask?
   c. If the oxide is supposed to be grown 1000 C, decide about wet or dry and calculate the time required for the oxidation.
1. A boron doped 111 Silicon wafer (N=1.0E16 /cm³) is being ion implanted with phosphorus at a dose of 1.0E16 /cm². If the implantation results in a projected range of 135 nm and a straggle of 53.5 nm and an average mobility of 1000 cm²/V.s,

a. What kind of a junction (P+N or N+P) is formed?

b. What is the maximum implant concentration in the implanted layer?

c. What is the resulting junction depth?

d. What is the sheet resistance of the implanted layer (state approximations/assumptions used)?

e. If a beam current of 100μA was swept over a square area of 10cm by 10cm how long a time would the process specified above take?

2. Describe the structure of an ion implanter and also answer the following:

a. What is the function of the electromagnet in an ion implanter?

b. How do you (1) generate, (2) extract and (3) accelerate the beam and make it dope (say) four wafers (4) uniformly?

c. If the beam is made up of positive ions and the wafers held at ground potential what polarity voltage would you apply to the source side of the accelerator?
1. Assume a square wafer of 12.5 cm x 12.5 cm size undergoes an IC process which results in 100 point defects uniformly distributed on it at the end. Determine, for each case below, how many good die and how much die yield this wafer/process combination would produce.

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<td></td>
<td></td>
</tr>
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2.a. What properties of Silicon make it better suited for integrated circuit fabrication compared to GaAs? Why?

2.b. Where does GaAs have advantage over Silicon? Why?

3.a. What is the meaning of “segregation coefficient”?

3.b. Explain (briefly) its effect on the Czochralski growth of Silicon.

3.c. Impurities A, B, C and D have the segregation coefficients in silicon, 0.01, 0.1, 1.0 and 10.0, respectively. A silicon crystal, after a float zone refinement process will be purified of which one(s)? Why?

4.1 A Czochralski grown silicon crystal shows a flower-like (daisy-like) bulging structure as viewed from the seed end. Think of crystal symmetry to answer the following questions.

a. If pattern appears to have four petals, what is the growth direction? and why?

b. If pattern appears to have six petals, what is the growth direction? and why?

4.2 Draw a unit cube representing a cubic crystal. Label the axes and show (112) and (013) planes on it.

**Diffusion/Oxidation Data:**
(hypothetical, for use in solving the following test problems only)

<table>
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<td>8.0E20 cm-3</td>
<td>1.2 E21 cm-3</td>
</tr>
</tbody>
</table>
5. A boron predeposition at 1000 C gives a dopant dose Q of 1E14 cm-2. It is followed by a drive-in diffusion of one hour at 1100 C. Find:
   a. the surface concentration after the predep,
   b. the time it took for the predeposition,
   c. the surface concentration after drive in, N(0), and
   d. the junction depth and the sheet resistance after all of these steps if the wafer were initially uniformly doped with phosphorous at 1E15 level.
   e. the junction depth if the initial doping were boron at 1E15 in (d)?

6. A boron doped 111 Silicon wafer (N=1.0E16 /cm3) is being ion implanted with phosphorus at a dose of 1.0E14 /cm2. If the implantation results in a projected range of 135 nm and a straggle of 53.5 nm,
   a. What is the maximum implant concentration in the implanted layer?
   c. What is the resulting junction depth?
   d. What is the sheet resistance of the implanted layer?
   e. If a beam current of 100uA was swept over a square area of 40cm by 40cm how long a time would the process specified above take?
   f. What is junction depth, peak concentration and the sheet resistance if the implantation is followed by a deep drive-in of 1 hour @ 1100 C.

3. A P-type doped wafer (1E16) and 1100 C 1Hr phosphorous diffusion is being used to make silicon N+P diodes.
   a. What is the junction depth?
   b. What is the oxide thickness needed to do an effective mask?
   c. If the oxide is supposed to be grown at 1050 C dry and calculate the time required for oxidation.